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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,886	09/30/2003	Hyunjun Kim	P16828	9223

7590 07/08/2008

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ART UNIT	PAPER NUMBER
2841	

MAIL DATE	DELIVERY MODE
07/08/2008	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HYUNJUN KIM, JIANGQI HE,

YUAN-LIANG LI, and PRASHANT PARMAR

Appeal 2008-0824
Application 10/674,886
Technology Center 2800

Decided: July 8, 2008

Before: JOSEPH F. RUGGIERO, MAHSHID D. SAADAT,
and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 (2002) from a rejection of claims 1-5, 7-16 and 18-21. No other claims are pending (Br. 2). We have jurisdiction under 35 U.S.C. § 6(b) (2002).

We affirm.

According to Appellants, the invention relates to a circuit board having first and second voltage planes, a signal layer on one side of the first voltage plane, and a plurality of microstrip line traces on the signal layer each electrically connected at one end to the second voltage layer. (Spec. 3-4, Figs. 1-2). The microstrip traces effect the overall impedance of the circuit board (*see* Spec. 1, 4). An understanding of the invention can be gleaned from exemplary claim 1, which is reproduced below:

1. An apparatus, comprising:

a first voltage plane having a first conducting portion to be at a first voltage;

a signal layer on one side of the first voltage plane;

a second voltage plane on the other side of the first voltage plane and having a second conducting portion to be at a second voltage; and

a plurality of floating microstrip line traces on the signal layer, wherein each microstrip line is (i) electrically connected to the second conducting portion at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion at the second end.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Tanahashi	US 6,172,305 B1	Jan. 9, 2001
Nibe	US 6,188,296 B1	Feb. 13, 2001
Janik	US 6,243,261 B1	June 5, 2001
Johnson	US 6,288,900 B1	Sept. 11, 2001

Claims 1-3, 5, 7-10, 12-16, 18 and 19 stand rejected under 35 U.S.C. § as being unpatentable over Tanahashi.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the collective teachings of Tanahashi and Nibe.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the collective teachings of Tanahashi and Johnson.

Claims 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the collective teachings of Tanahashi, Janik and Johnson.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Brief and the Answer for their respective details.[1] In this decision, we have considered only those arguments actually made by Appellants. Appellants' arguments call attention to the fact that the appealed claims recite "a first voltage plane," "a second voltage plane," and "a plurality of floating microstrip line traces" (Br. 4, 5), features which are present or similarly present in each of the appealed independent claims 1, 14, 18, and 20. Accordingly, we select claim 1 as representative of the group of claims 1-3, 5, 7-10, 12-16, 18 and 19.

Arguments which Appellants could have made but did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

The issue is whether the Appellants have demonstrated that the Examiner erred in determining that Tanahashi renders claim 1 obvious.

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[1] We refer to the Brief filed Nov. 7, 2006 ("Br."), and the Answer mailed Mar. 26, 2007 ("Ans.").

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious without an explicit application of the teaching, suggestion, motivation test.

In particular, the Supreme Court stated that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The Court explained:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a

> technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 1740. The operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

Under this framework, once an Examiner demonstrates that the elements are known in the prior art and that one of ordinary skill could combine the elements as claimed by known methods and would recognize that the capabilities or functions of the combination are predictable, then the Examiner has made a prima facie case that the claimed subject matter is likely to be obvious. The burden then shifts to the Appellants to show that the Examiner erred in these findings or to provide other evidence to show that the claimed subject matter would have been nonobvious.

"[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR.*, 127 S. Ct. at 1741 (citing *In re Kahn*, 441 F.3d at 988).

ANALYSIS

Regarding claim 1, Appellants' disputes focus on the Examiner's determination that Tanahashi teaches voltage *planes* and a *plurality* of microstrip line traces (Ans. 4-7, Br. 4-5).

As to the voltage planes, the Examiner found that Tanahashi's insulating layers l1 and l2 having wiring conductors P2 and G1 thereon (Figs. 3A-3C) constitute voltage planes having conductive portions meeting the claim (Ans. 4). Appellants respond that the conductor P2 on layer l2 is not a voltage plane because "neither P2 nor layer l2 is a level of the circuit board dedicated to a voltage level (*e.g.*, a ground plane or a + 5.0 volt plane). Indeed, in addition to P2, layer l2 includes ground G2 (see FIG. 3C of Tanahashi)." (Br. 4-5).

We are in general agreement with the Examiner. We determine that a portion of P2 constitutes a first conducting portion of a voltage plane P2 at a first voltage, and likewise, a portion of G1 constitutes a second conducting portion of a second voltage plane G1 at a second voltage.[2] (*See* Tanahashi, Figs. 3A-3C). We find the Examiner's reasoning to be sound: "Applicant has provided no specific special definition to the term 'first voltage plane' and further that in determining the broadest reasonable interpretation of the term 'first voltage plane' consistent with the specification, the ordinarily skilled artisan would define 'first voltage plane' as simply a first plane, which provides a voltage." (Ans. 9).

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[2] Power wiring conductor P2 and ground wiring conductor G1 are clearly depicted at Figure 3A to be planar layers; moreover, as disclosed capacitances, they have planar opposed areas (*see* col. 14, ll. 31-43, s*ee also* Tanahashi, Figs. 3B, 3C). While we determine that P2 and G1 constitute the claimed voltage planes, we also alternatively agree with the Examiner's position that insulating layers l1 and l2 constitute portions of the voltage planes (*see* Ans. 9). The claim, reciting "a first voltage plane having a first conducting portion" reasonably contemplates, and at a minimum, does not preclude, another non-conducting portion, such as insulating portion L2, as the Examiner determined.

We are not persuaded by Appellants' argument quoted *supra* that power conductor P2 is not dedicated to a single voltage level (*see also* Br. 5, n. 1). Relative to ground conductor G1 dedicated to a ground (second) voltage level, P2 is dedicated to the single power supply (first) voltage level (*see* col. 6, ll. 17-24, col. 13, ll. 28-55). Similarly, Appellants' argument that insulating layer l2 is not dedicated to a single voltage is not persuasive because Appellants' disclosed first voltage plane, like Tanahashi's layer l2, has at least two voltage levels. That is, Appellants' disclosed first voltage plane located on top of layer 210 comprises both a first conducting portion 220 with a first voltage and a section of plated connection 250 with a second voltage (i.e., plated through hole connection 250 is electrically connected to the second voltage plane 230 at a second voltage level). Additionally, the hole 260 constitutes a third voltage level. (*See* Spec. 3:25 to 4:6; Fig. 2).

Thus, we find that Tanahashi's power wiring conductor P2 and ground wiring conductor G1 respectively constitute first and second voltage planes having first and second conducting portions at first and second voltage levels in the manner claimed. Consequently, Appellants have not convinced us of error in the Examiner's determination that Tanahashi teaches the claimed voltage planes.

The final dispute on appeal is over the claimed "*plurality* of floating microstrip line traces on the signal layer." (Cl. 1, emphasis added). Appellants do not dispute the Examiner's finding that layer G4 constitutes one of the claimed plurality of traces on the signal layer l4 (Ans. 4, Br. 5; Tanahashi, Figs. 3A-3C). This final dispute is specifically over whether

Tanahashi's disclosure at column 16, lines 51-61 fairly teaches plural traces on the signal layer l4 (Ans. 10-11, Br. 5). Appellants contend that the teaching is limited to additional traces on additional circuit board insulating layers to be added to the existing depicted insulating layers l1 to l4 (Figs. 3A-3C), and therefore does not apply to the existing signal layer l4 as the Examiner found (Br. 5). Again, we agree with the Examiner.

The disputed Tanahshi passage follows:

> The multilayer circuit board according to the invention, in each of the above embodiments, may comprise an insulating substrate under the first insulating layer I1, and may comprise another insulating layer so as *to cover the fourth insulating layer l4 and the respective wiring conductors placed thereon.* Further, *a plurality of wiring conductors may be placed for each kind*, and various multilayer circuit boards configured by the first to fourth insulating layers l1 to l4 may be combined and overlaid on the multilayer circuit board configured by the first to fourth insulating layers l1 to l4.

(col. 16, ll. 51-61) (emphasis added).

We find that "a plurality of wiring conductors may be placed for each kind" refers to the several different kinds of "wiring conductors" in general (i.e., G1-G4, P1-P4, S1-S2), including those on the fourth insulating layer l4 (such as G4) specifically referred to in the passage above. Therefore, Tanahashi fairly and reasonably teaches another wiring conductor (i.e., trace) such as another trace like G4 on signal layer l4, constituting "a plurality of floating microstrip line traces," as the Examiner determined (Ans. 4, 10-11). Consequently, Appellants have not convinced us of error in the Examiner's position.

Finally, we turn to Appellants' statement which is related (tangentially) to the dispute over the plurality of traces: "Nor would the use of multiple floating traces and voltage planes as recited in the claims be obvious in view of Tanahshi. By configuring the floating traces and voltage planes as recited in the claims, an overall impedance associated with a circuit board may be damped and the efficiency of the power delivery system may be improved." (Br. 5) (citation omitted). Such a conclusory statement only highlights asserted benefits of the claimed invention, but points to no error in the Examiner's specific finding that "it would have been obvious . . . to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. . . . to ensure that each line is at the same voltage, thus avoiding any unwanted current flow" (Ans. 4). Since Appellants' statement does not amount to any argument asserting an error, Appellants have not met the burden on appeal of asserting error regarding the Examiner's reason for modifying Tanahashi's teaching of a second trace to be connected in the manner claimed.

While the Examiner's reason for modifying Tanahashi has not been challenged, we nonetheless find it to be supported. Tanahashi's invention is directed to symmetrically opposed planar circuit board traces which beneficially increase the capacitance and decrease the overall circuit board characteristic impedance (col. 2, l. 59 to col. 3, l. 3; col. 5, l. 53 to col. 6, l. 24; col. 14, ll. 12-17, 31-43; Figs. 3A-3C). Thus, one of ordinary skill in the art would have recognized that Tanahashi's teaching of additional planar conductors for each type, quoted *supra*, suggests attaching the additional

conductors in a manner that mimics the existing wiring layer structure, in congruence with the Examiner's reasoning (*compare* Ans. 4-5).

Moreover, additional side-by-side wiring conductors connected electrically in parallel predictably would render Tanahashi's desired increased capacitance benefit, while also ensuring integrity based not only on the well known principle of redundancy, but also based on the well known related benefit rendered by the inherent division of current flow among the additional side-by-side conductors; i.e., the benefit being the decreased likelihood of a wire break/burn due to excessive power. Thus, two planar, closely spaced, side-by-side wires of the same area as a single existing planar wire, would have rendered essentially the same capacitance and symmetry as the single wire, but also predictably and beneficially would have provided increased circuit integrity. On the other hand, increasing the total overlapping area with one or more additional underlying wire(s) further would have increased the capacitance, as well as the circuit integrity, predictably and beneficially.[3]

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[3] We also alternatively determine that the layer P4 (Fig. 3A) constitutes another floating microstrip line trace, which, in conjunction with trace G4, meets a plurality of such traces in the manner claimed. We find that all the power lines and ground lines (P1-P4, G1-G4) are ultimately, implicitly connected together to one power source, or at a minimum, suggested to be connected electrically together via the power source and semiconductor devices of the circuit where such a connection beneficially decreases the circuit board characteristic impedance and stabilizes the power supply and semiconductor device (*see* col. 4, ll. 51-53, col. 6, ll. 17-24; col. 14, ll. 31-43). Thus, in this scenario, trace P4 would be electrically connected to second voltage plane conducting portion G1 at each P4 trace end (which

In summary, we find that a skilled artisan, applying the teachings of Takashani in light of well-known elementary principles, would have arrived at the claimed invention to obtain the beneficial results of increased capacitance and integrity, and decreased impedance. Accordingly, Appellants have not persuaded us of error in the Examiner's conclusion of obviousness.

For the reasons outlined above, we will sustain the rejection of independent claim 1. Since Appellants have not argued separately claims 2, 3, 5, 7-10, 12-16, 18 and 19, we also will sustain the rejection of those claims for the same reasons. Likewise, we will sustain the different rejections of claims 4, 11, 20 and 21 which also have not been argued separately. (*See* Br. 4).

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includes the P4 first trace end at T5), but not directly connected to any other microstrip line trace (such as G4) or to the second conducting portion G1at the P4 second trace end (the uppermost end in Figure 3A of trace P4) - meeting the claim.

Similarly, we additionally and alternatively determine that connecting multiple circuits together on the same circuit board levels l1 to l4 would meet the claim because two microstrip traces G4 in different circuits would then be on the same signal level l4 and connected in the manner claimed. We find that the disputed passage of Tanashani quoted *supra* not only teaches connecting similar circuits on different levels together (as implicitly agreed upon by Appellants and the Examiner (*see* Br. 5, Ans. 11), but it also suggests connecting plural similar circuits on the same levels l1 to l4. Such multiply connected similar circuits would have predictably and beneficially rendered a more densely populated compact device.

CONCLUSION

Appellants have failed to persuade us of error in the Examiner's rejections. *See In re Kahn*, 441 F.3d at 985-86.

Accordingly, we sustain the Examiner's rejections of claims 1-5, 7-16, and 18-21.

DECISION

The decision of the Examiner is *affirmed*.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED

KIS

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